SECOND QUARTERLY REPORT

DEVELOPMENT OF CADMIUM SULFIDE THIN FILM PHOTOVOLTAIC CELLS

BY

F. A. SHIRLAND, F. AUGUSTINE, and W. K. BOWER

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

CONTRACT NAS 3-6461

MAY 12, 1965

GPO PRICE $ _____

OTS PRICE(S) $ _____

Hard copy (HC) $2.00

Microfiche (MF) .50

ELECTRONIC RESEARCH DIVISION

CLEVITE CORPORATION

SECOND QUARTERLY REPORT

DEVELOPMENT OF THIN FILM CdS PHOTOVOLTAIC CELLS

by

F. A. Shirland, F. Augustine and W. K. Bower

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

May 12, 1965

CONTRACT NAS 3-6461

Technical Management
NASA Lewis Research Center
Cleveland, Ohio
Space Power Systems Division
L. R. Scudder

CLEVITE CORPORATION
Electronic Research Division
540 East 105th Street
Cleveland, Ohio 44108

TABLE OF CONTENTS

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

LIST OF ILLUSTRATIONS

LIST OF TABLES

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

DEVELOPMENT OF THIN FILM CdS PHOTOVOLTAIC CELLS

Second Quarterly Report
January 15 through April 14, 1965

Contract No. NAS3-6461

N5462 over

INTRODUCTION AND SUMMARY

The objective of the presently reported phase of the program is the development of high efficiency large area plastic substrate thin film CdS solar cells. In addition the use of very thin CdS films for large area cells is being attempted, and selected improvements in the design of frontwall metal substrate CdS thin film cells are being made.

In this period steady improvements were effected in the process for making frontwall plastic substrate cells. In particular, an improved conductive coating for the plastic was developed, and this has led to higher efficiencies. Three cells of 3" x 3" size with initial efficiencies over 4% were obtained. The average efficiency of the 22 large area plastic substrate cells fabricated in the quarter was 3.0%.

Six of eleven smaller area cells fabricated had more than 5.0% efficiency, and two cells of 7 cm^2 area had 5.8% efficiency. It has become evident that there is a definite area effect on these cells which shows up in the short circuit current density. It has been found that this area effect results from some unidentified aspect of the processing of the cell rather than from the area per se.

A study of the effect of various CdS doping levels on the characteristics of the evaporated films was completed. The composition and evaporation parameters for each layer of the double layer film can now be specified. The study of the effect of the thickness of each layer on cell characteristics has been started. Tooling for the evaporation of very thin films was completed and proven in.

Additional test data from the vacuum thermal cycling of various design film cells have been obtained from NASA, Lewis Research Center. The frontwall metal substrate cells with conductive epoxy cemented grids

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

showed no shorting, but they did degrade severely. The degradation shows the pattern that has become associated with moisture or impurity contamination, so there is hope that it can be eliminated. Two plastic substrate cells, while of low efficiency initially, have shown no shorting or appreciable degradation up to 1500 cycles.

DOUBLE LAYER FILM STUDY

The use of a nonconducting plastic substrate requires that the CdS film itself be very conductive, otherwise the losses due to the sheet resistance of the CdS film become excessive for larger area thin film cells. But only very low voltage cells can be fabricated from suitable highly conducting CdS films. If, however, a highly conducting CdS film is deposited on the insulating substrate and followed by a second poorly conducting CdS layer on which the barrier is subsequently formed, it should be possible to have the advantages of both extremes in a single film. This is the idea of the double layer, which is similar in principle to the tailoring concept of Aldrich and Cusano. [1]

Double layer films can be secured in several ways. Aldrich and Cusano add a selected impurity dopant towards the end of film formation to compensate the charge carriers. This is readily done in the case of their CdTe films because the charge material is continuously fed into a reaction chamber where flash evaporation occurs. CdS films are usually formed from fixed composition material precharged into cylindrical evaporation sources. Thus in this case it is more convenient to use differently doped material in some of the evaporation sources and to fire the sources sequentially.

As discussed in the First Quarterly Report the initial attempts were to deposit a 15 micron thick film of highly doped CdS of nominal 0.01 ohm-cm resistivity, followed by a second 15 micron thick layer of undoped CdS of nominal 100 ohm-cm resistivity. These first double layer films did not yield very good cells and on investigation extreme variability was found in the properties of the films. Hence, the characteristics of low and of high resistivity single layer films were studied separately in an effort to get these under better control.

2

a. <u>Indium Doped Films</u>

A series of films were evaporated onto insulating lapped glass substrates using various amounts of indium (up to 1 mol%) presintered into the starting charge material. The electrical resistivity and optical transmission of these films were measured and are plotted in Figs. 1 and 2 respectively.

An essentially linear relationship in the log-log plot of resistivity vs. indium in the charge is evident for dopings up to 0.1 mol%. At higher levels the resistivity is considerably less than expected from an extension of the line established for the lower levels. This is probably because a smaller proportion of the total indium content carried over into the deposited films at these higher impurity levels.

A resistivity of 230 ohm-cm was measured on a film of this series with no indium in the charge material. If the line of Fig. 1 is extrapolated to 230 ohm-cm it corresponds to 0.00025 mol% indium, or 2.5 parts per million. This seems to be a reasonable value for the residual donor impurities to be expected in an undoped CdS film.

The transmission of light through these CdS films is plotted in Fig. 2 against the amount of indium dopant in the charge material. The transmission was calculated from the current output of a standard silicon solar cell when the sample CdS film was inserted between the silicon cell and a tungsten light source, as compared with the output with only a glass substrate inserted between cell and light source. There was a 31% loss in transmission for the undoped CdS film on a lapped glass substrate as compared with just the glass substrate. This seems high, especially for tungsten lamp illumination. In an actual cell there would be better optical coupling between the various layers so that more of the light would reach the active barrier region of the backwall cell than indicated from these data.

However, the relationship of interest here is relative rather than absolute. From 0 to 0.1 mol% indium in the starting charge material the transmission through a 1 mil thick CdS film is reduced from 69% to 57% at an approximately linear rate. The points for 0.5 and 1.0 mol% indium were at 48.8 and 48.6% transmission respectively. This is

3
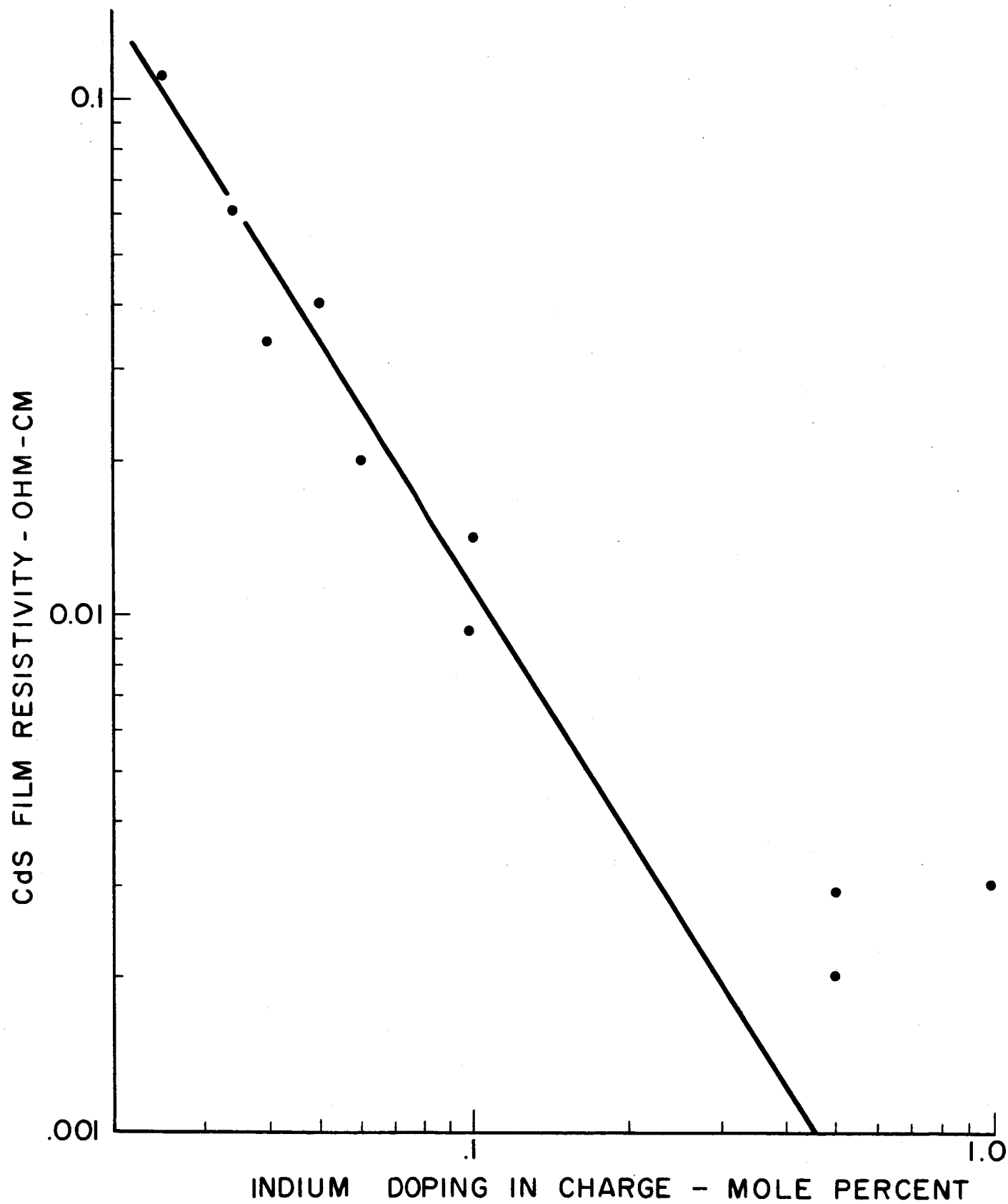
FIG. I. EFFECT OF INDIUM DOPING ON RESISTIVITY

4
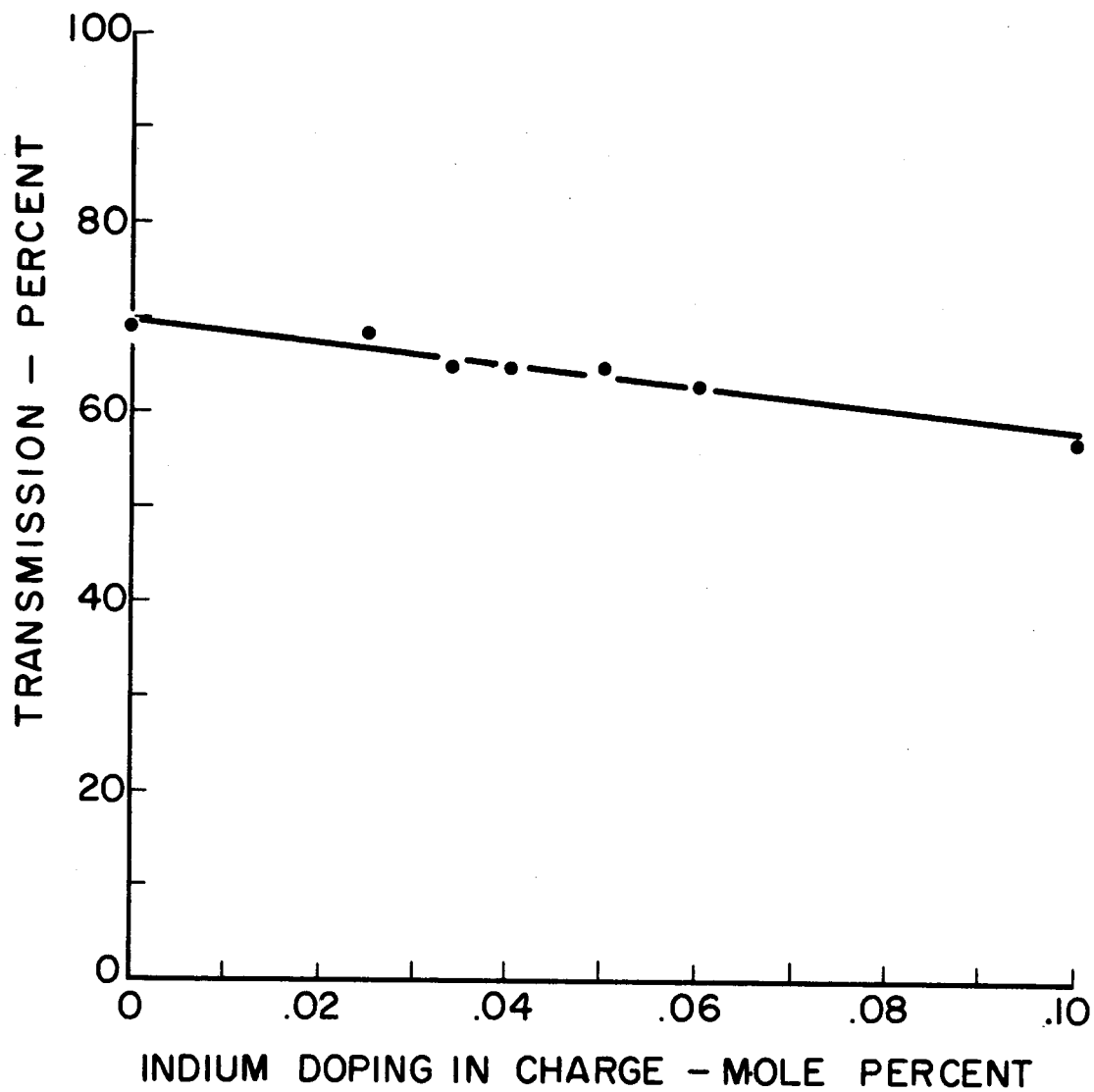
FIG. 2. EFFECT OF DOPING LEVEL ON TRANSMISSION

5

considerably higher than would be expected from an extrapolation of the line in Fig. 2. As in the case of the resistivity for these two high levels of indium doping, the explanation probably is that the indium content of the films fell far short of that of the starting charges.

Initially, at least, the intent is to work with resistivity levels in the range of 0.01 ohm-cm for the lower layer of the double layer films. Thus, indium doping levels of 0.1 mol% are indicated, though the level may change slightly for different lots of CdS raw material. At this doping level about a 12% penalty may result in output of a backwall cell due to increased absorption in the CdS layer. This however would be off-set by a decrease in the losses due to the sheet resistance of the CdS layer.

At present this appears to be a reasonable compromise between the conflicting requirements of transmission and conductivity. Optimization of these factors cannot be done until the geometry of the double layer film is specified, and this in turn depends on what minimum film thicknesses are found to be required for the high and low resistivity CdS layers.

From these considerations, it appears that indium doped CdS will probably be quite satisfactory for the lower layer (next to the substrate) of double layer films.

b. Undoped Films

On the basis of several earlier measurements, it was expected that undoped CdS films would have resistivities on the order of 100 ohm-cm when formed under the standard evaporation conditions, and that the cells fabricated from such films would have open circuit voltages of about 0.48 to 0.50 volts. A number of double layer films were made using 0.1 mol% indium doped material for the lower layer and undoped material for the upper layer. However, cells fabricated from these films had lower voltages than expected.

Because the presence of the highly conducting lower layer prevents accurate measurement of the resistivity of the upper layer, a number of evaporations of undoped CdS charge material were made on insulating glass substrates. A wide variation was found in the resistivities

6

of these films. Additional measurements taken on test plates inserted near the substrates during standard evaporations in both of the 18" evaporators, using a number of lots of sintered (undoped) CdS material, confirmed the wide variation. In nearly 50 such tests the resistivity of the films varied from as low as 0.9 ohm-cm to as much as 260 ohm-cm, though most of the films were less than 20 ohm-cm.

There appeared to be no relationship between film resistivity and the evaporator used, nor was the variation within a single lot of CdS material very much less than that between lots, though it was somewhat less.

Several suspected major causes for the resistivity variation were investigated. The first of these was the possible contamination of the films from the tooling used in the evaporation chamber. The various heat shields, masks, etc. in the vacuum chamber get coated with CdS and are cleaned periodically (but not after each evaporation) by soaking in HCl. It was noted that the resistivities of the CdS films evaporated right after the periodic cleanings were generally lower than those run after several intervening evaporations without cleaning the system.

Analysis of films evaporated right after the tooling had been cleaned did disclose heavy iron contamination. Special precautions to remove the residues left on the tooling after cleaning (by polishing, rinsing, etc.), reduced the effect but did not eliminate it altogether.

Another cause of resistivity variation might result from changes in the rate of evaporation of the charge material. While the substrate temperature can be controlled reasonably accurately, it is much more difficult to control the temperature of the evaporation sources. Source temperature is presently controlled by monitoring the color of the tubular tantalum sources with an optical pyrometer and making adjustments in the current through the sources. However, it is known that the temperature inside the sources is very much higher than that measured by the color of the external surface. On at least two occasions nickel screens, used as baffles inside the sources, melted (nickel melts at about 1455°C) during runs where the outside source temperature did not exceed 1050°C.

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

An attempt is being made to secure a suitable commercial rate monitor, so that better control can be exercised over this factor. In the meantime, some indications were obtained through the use of a special design sequential stepping shield. This permitted exposing a portion of a substrate to the evaporation stream for up to eight selected fractions of the total cycle. Thus the amount evaporated during say the first, second, ..., etc., to the eighth minutes could be collected and the average deposition rate for each of the eight periods calculated.

A number of such calibrations disclosed that there were indeed some variations in deposition rate throughout the evaporation period, and these were correlated to the age of the evaporation sources. It was found that during about the first 16 runs on a set of evaporation sources the deposition rate was reasonably uniform throughout the entire evaporation cycle, and that the variation in rate from run to run was minor. However, after about 15 runs from a set of sources, there was an increasing tendency towards a "quick blast" type of evaporation with the rate increasing to as much as double the normal rate for the first 8 or 10 minutes and dropping to about a third the normal rate for the remaining portion of the cycle.

We were not successful in correlating this behavior with the resistivity variation of the resulting films, nor with the characteristics of the cells made from the films. However, such variation can hardly be conducive to obtaining uniform films. It is expected that a rate monitor will help in this respect. In the meantime the use of older evaporation sources is being avoided.

This investigation has not been completely successful in enabling uniform undoped CdS films to be formed at the presently desired 100 ohm-cm resistivity level. However, it has been possible to pin-point and eliminate some causes of variation. It does appear that average film resistivity is still somewhat below the 100 ohm-cm level, even with the improvements. Adjustment upwards might be effected in several ways including: counter-doping with acceptor type impurities, decreasing the evaporation rate, increasing the substrate temperature, or by post annealing the films in a sulfur atmosphere. The first of these seemed most practical.

c. Copper Counter-Doped Films

Several evaporations were carried out using copper added to the starting material in an attempt to partially compensate the residual donor impurities in the CdS and the sulfur vacancies grown into the deposited films. The first attempt was to use CdS material to which 5 parts per million of copper, as cupric chloride, was added prior to sintering. Two films on insulating glass substrates gave resistivities of 130 and 208 ohm-cm. This is appreciably higher than the average resistivity for undoped films formed under the same evaporation conditions, but still within the range of variability for undoped films.

A single layer CdS film was evaporated using 5 ppm copper counter-doped CdS starting material and a standard molybdenum foil substrate. The resulting film was 1.0 mils thick, which was slightly higher than the average CdS film thickness in use at the time. The 3" x 3" frontwall cell fabricated from this film had an OCV of 0.47 volts, an SCC of 17 mA/cm^2 and a conversion efficiency of 4.9%. This level of voltage, current, and efficiency was not discernibly different from the standard pilot line cells made at the same time from undoped CdS films. It is of interest that a test strip evaporated on glass at the same time as the above molybdenum substrate film had a resistivity of only 23 ohm-cm.

Though these three films do indicate that slightly higher average resistivity may be obtained by the use of about 5 ppm of copper in the charge material; a larger effect was anticipated and is still desired. Therefore, a much more heavily copper doped material was tried. An ingot of single crystal vapor phase grown CdS containing 1% of copper (as cuprous sulfide) was obtained from the Electronic Research Division Semiconductor Section. This material was of very high resistivity ($>> 10^6$ ohm-cm). It was crushed to powder and used as the charge material for a film evaporated onto an insulating glass substrate. The film resistivity was only 149 ohm-cm. Thus, it appears that counter doping of CdS by the use of copper in the starting material will yield only a slight increase in the resistivity of vacuum evaporated films.

Much greater increases in resistivity can be achieved by the use of higher substrate temperatures.

d. Double Layer Film Cells

On the basis of the conditions established for the evaporation of indium doped CdS material to obtain 0.01 ohm-cm resistivity films, and undoped CdS for higher resistivity films, a few double layer films were deposited on molybdenum substrates and processed into cells. Five cells were fabricated. The results on these cells were somewhat poorer than is being experienced on regular single layer CdS film cells on molybdenum substrates of comparable size.

From an analysis of the I-V characteristic curves it is found that while the open circuit voltage is about the same for these double layer film cells as for the standard single layer film cells, the short circuit current density is slightly lower and the fill factor is also lower. In each case there appears to be more series resistance to these cells. The data are listed in Table I.

The thickness of these films is about the same or slightly higher than for standard single layer cells, so the lower output cannot be ascribed to this factor. There is one factor that was appreciably different in the processing of these double layer films. The deposition rate was much less because the CdS material was evaporated half from two sources and then half from another two sources rather than from all four sources simultaneously. Thus the net deposition rate was about half that normally experienced. This could well have changed the structure of the films sufficiently to lead to the differences in cell characteristics that were actually experienced.

VERY THIN FILM STUDY

a. Introduction

The detailed quantitative mechanism of the photovoltaic effect in CdS is still a matter of some controversy. There is however a fair amount of agreement on the major constructional features of the cell. The barrier layer appears to consist of, very roughly, about

10

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

TABLE I

DOUBLE LAYER CdS FILM CELLS ON MOLYBDENUM SUBSTRATES

Cell No.	Evaporation Time	Subst. Temp. °C	Film Thick (mils)	OCV (V)	SCC (mA/cm^2)	Fill (%)	Eff. (%)
A-461	20 min - doped layer 5 min - shutter closed 20 min - undoped layer	220 220-250 250	0.9	0.455	18.9	55	4.85
A-475	20 min - doped layer 5 min - shutter closed 20 min - undoped layer	220 220-300 300	0.95	0.465	13.2	56	3.0
A-480	18 min - doped layer 2 min - overlap 23 min - undoped layer	220 220 220	1.0	0.46	16.7	53	4.15
A-485	20 min - doped layer 5 min - overlap 20 min - undoped	220 220-300 300	1.1	0.48	14.8	55	3.95
A-488	20 min - doped layer 5 min - overlap 20 min - undoped layer	220 220 220	0.9	0.47	13.5	56	3.2

Note: Cell A-461 was 1 1/2" x 1 1/2" area, others were 3" x 3".
Doped layer in each case was evaporated from 0.1% indium doped charge material.

11

0. 1 microns thickness of a semicontinuous layer of some form of Cu_2S formed directly on the CdS. The depletion region probably extends into the CdS. From capacitance measurements it is believed to be no more than a few tenths microns in thickness. Cuprous ions may diffuse into the CdS lattice, probably in association with a donor impurity or a lattice defect, to form photon absorption centers and electron trapping sites, but these probably do not penetrate the CdS surface beyond a few hundredths of a micron.

From the above it would appear that the active portions of the CdS solar cell are very thin indeed, but it is not known just how much CdS is really required for a practical solar cell. Some years ago one of the author's work at another laboratory indicated that for 3" x 3" size film cells the CdS layer should be on the order of 50 microns in thickness.[2] For thinner CdS films, low efficiency cells with poor I-V characteristics were encountered as an appreciable proportion of the cells processed. However, even at that time some cells fabricated from CdS films as thin as 20 to 25 microns gave cell efficiencies as high as the thicker CdS films.

Since that time, Shirland, Hietanen and Bower, on a Clevite in-house program, developed an improved CdS film deposition and solar cell fabrication process, whereby CdS films of 15 to 25 microns thickness were used to fabricate cells of 4 to 6% sunlight conversion efficiencies in 3" x 3" sizes. Very few low output cells were encountered, and the difficulties generally seemed more associated with series resistance than with shunt leakage effects.

Chamberlin, et al.,[3] on an Air Force sponsored project, succeeded in fabricating CdS solar cells of a few percent efficiency and a few square centimeters area using CdS films as thin as 1 micron. The films were formed by a thermal decomposition process rather than by vacuum evaporation. The barrier layer was also formed by thermal decomposition.

In view of the above it is strongly suspected that a micron of CdS would be sufficient thickness for a solar cell if the film were perfect enough to keep the substrate physically separated from the barrier layer,

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

and if the shorting paths along CdS grain boundaries were minimized.
If such thin CdS films could be used, the substrate thickness could also
be very thin, on the same order, and hence extremely thin, flexible
CdS solar cells with very high specific power to weight ratios might be
realized. It is one of the objectives of the present contract to study the
possibility of using very thin CdS films, on the order of 1 to 3 microns
thickness, for practical large area solar cells.

The approach being followed is to secure higher perfection
films by the use of much higher substrate temperatures and lower deposi-
tion rates. It is recognized that films formed from undoped CdS at very
high substrate temperatures will be very high in resistance and it is
expected that deliberate donor doping will be required.

The initial work on the very thin films has been largely
exploratory to determine the kind of tooling required for securing thin
films at high substrate temperatures and to see what kinds of problems
will be encountered.

b. Preliminary Trials, Open Chamber Evaporation

The first trials with higher substrate temperatures were
made using an open evaporation chamber and undoped CdS starting
material. At 400°C substrate temperature, a film about 3.7 microns
thick was secured on an insulating glass substrate that had a resistivity
of 550 ohm-cm. This film was a very light straw yellow in color and
visually appeared to be homogeneous and free from pin holes or spatter.
It was highly photoconducting.

Another film evaporated onto a molybdenum substrate held
at 400°C temperature was only 1.2 microns thick and also appeared
homogeneous and free from flaws. It was attempted to process this
film into a cell, but a dead short was obtained.

An exploratory series of films was prepared on insulating
glass substrates in an open evaporation chamber using undoped CdS and
various substrate temperatures from 220°C up to 570°C. Table II sum-
marizes the measurements taken on these films. All of the films
looked homogeneous and free from pin holes and spatter.

13

TABLE II

PROPERTIES OF CdS FILMS FORMED AT VARIOUS
SUBSTRATE TEMPERATURES

Film No.	Substrate Temperature	Film Thickness	Resistivity	Transmission
	°C	(micron)	(ohm-cm)	(%)
C-1	220	20	141	-.-
C-2	220	17.5	126	68.5
C-3	220	20	32	68.0
C-4	400	3.8	27,000	76.5
C-6	400	3.0	31,000	66.5
C-5	570	0.5	690,000	70.5

Note: Vycor substrates.

Undoped CdS starting material.

All films were pale yellow in color, pin hole and spatter free, and uniform in thickness.

14

Initial attempts to form films on Vycor substrates at temperatures of 600°C were unsuccessful as the CdS films which deposited on the substrates re-evaporated before they could be cooled and removed from the vacuum chamber. Substituting molybdenum foil substrates for the Vycor did not keep the deposited CdS from re-evaporating, even when the substrate temperature was lowered to 550°C. Several attempts gave the same results.

It was noticed that on these trials with molybdenum foil substrates, there was a large dark blue spot-like discoloration of the molybdenum where the CdS re-evaporated from the substrate. At first this was thought to be oxidation occurring due to reaction of residual oxygen in the chamber with the molybdenum held at the elevated temperature. When the system was flushed several times with helium, prior to heating the substrate and evaporating, there was no change in the amount of this discoloration.

It was noted that the discoloration occurs not when the substrate is heated in the vacuum chamber, but only when the CdS evaporation begins. Thus it seems fairly evident that it is some form of molybdenum sulfide. The layer is very thin, very conductive and does not seem to harm the adhesion of the CdS film subsequently deposited on it. In view of these factors no further effort was placed on trying to identify or eliminate this discoloration, though the condition is being watched to make sure that no harmful effects do occur.

c. Hot Wall, Closed Chamber Evaporation

Further work on the very thin films was done using the hot wall semi-closed chamber technique. The arrangement of the tooling is shown in Fig. 3. The hot wall was a quartz cylinder 1 1/2" in inside diameter, open at both ends. It has a tantalum heater wound around the outer surface which in turn is wrapped with a layer of "Fiberfrax" insulation as a heat shield. The hot wall is positioned over the single evaporation source and extends to the substrate. The source to substrate distance is 5 1/2".

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

SUBSTRATE
HEATER

THERMOCOUPLE

SUBSTRATE

INNER CHAMBER
(QUARTZ)

HEATER COILS

INSULATION
HEAT SHIELD

THERMOCOUPLE

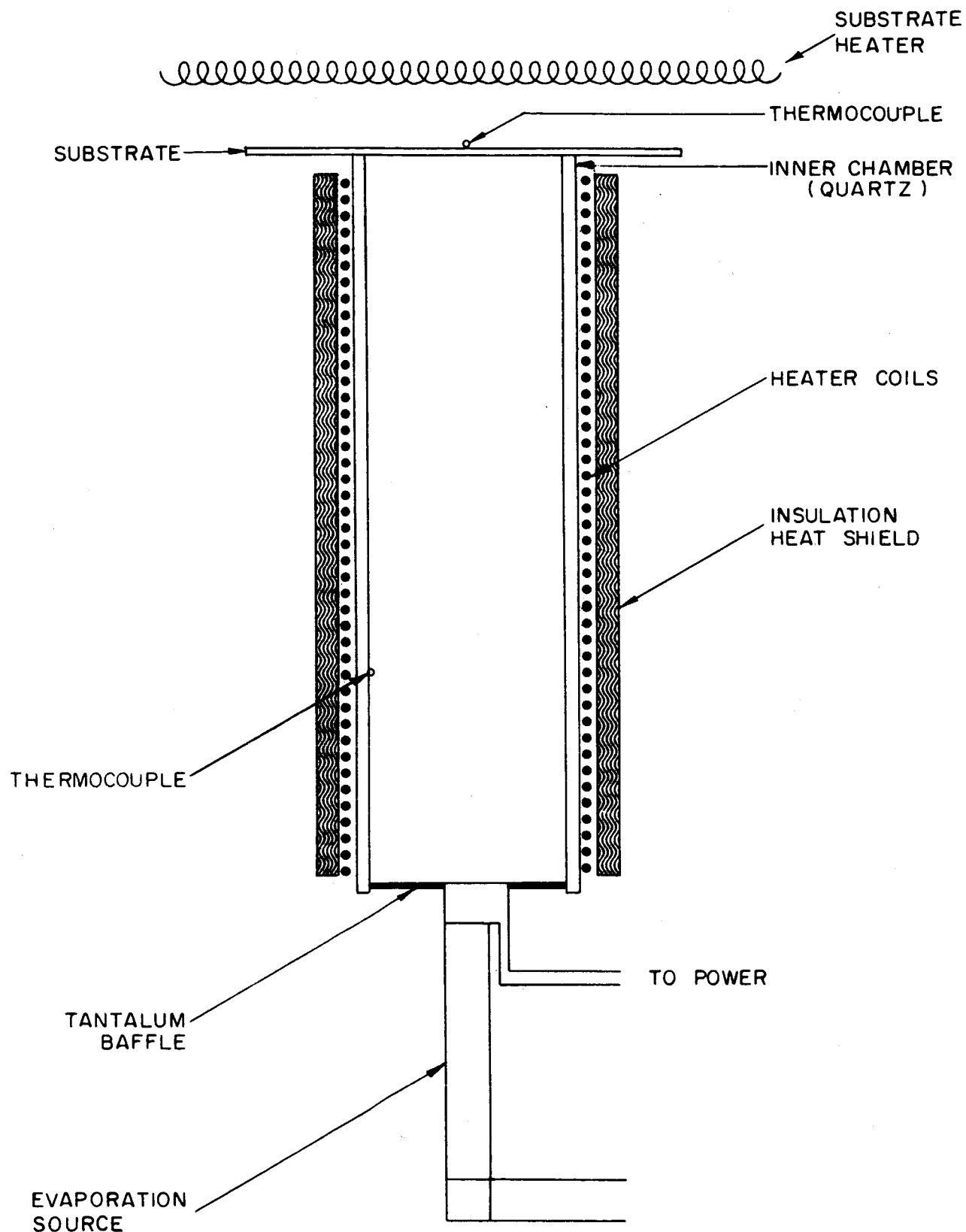TO POWER

TANTALUM
BAFFLE

EVAPORATION
SOURCE

FIG. 3.   TOOLING FOR EVAPORATION OF CdS FILMS AT
HIGH SUBSTRATE TEMPERATURES.

16

The first evaporations carried out at temperatures of 600° substrate temperature and 650°C wall temperature were done with a 1/4" gap between the top of the inner cylinder and the substrate, and with the bottom of the cylinder open. It was found that in order to get any deposition on the substrate the inner cylinder had to be closed, as shown in Fig. 3. Then, with 5 gram charges in the source, a source temperature of 1085°C, and substrate temperatures in the range of 400 to 600°C, very thick large grained films were obtained. These were runs C-23 to C-25 as listed in Table III.

When the charge was reduced to about 1 gram of CdS, thinner films, in the range of 10 to 40 microns, were obtained (runs C-26 to C-29). However, these films were not of uniform thickness. They tended to be thin in the center and thick around the outer edges. It seems probable that the center of the substrate is receiving additional radiation from the hot wall which may cause a temperature gradient that in turn might cause the nonuniform deposition of CdS. However, sufficient temperature gradient to account for the difference in film thickness actually experienced was not detected when the back surface of the substrate was probed with a thermocouple.

Films C-27 and C-29 were processed through barrier formation and probed for voltage output under 100 mW/cm^2 tungsten light. Cell C-27 gave 0.35 volts (open circuit) from the 7 micron thick area, and 0.45 volts from the 15 micron thick area. Cell C-29 gave an output of 0.42 volts from both the inner (thin) and outer (thick) regions. These voltages are in line with normal experience on standard frontwall metal substrate cells at this stage of processing.

BACKWALL PLASTIC SUBSTRATE CELL

The efforts to fabricate large area backwall plastic substrate cells were continued for awhile in the second quarterly period. A "standard" laboratory cell fabrication line was set-up and operated. However, the lack of a suitable standard process prevented any reproducible results. As discussed previously, the problem was still the collection of current from the n-region of the CdS film. Efforts were therefore put onto the use of grids under the CdS layer.

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

TABLE III

HIGH TEMPERATURE CdS FILM EVAPORATIONS USING HOT WALL CLOSED CHAMBER TECHNIQUE

Film No.	Substrate Temperature °C	Wall Temperature °C	Film Thickness (micron)	Remarks
C-23	400	500	> 250	large grained film, poor adherence, little spatter
C-24	500	600	250	large grains, poor adherence, little spatter
C-25	600	700	150	medium grains, poor adherence, no visible spatter
C-26	600	700	31	fine grains, good adherence, no visible spatter
C-27	600	700	7-15	fine grains, good adherence, no visible spatter
C-29	600	700	13-38	fine grains, poor adherence, no visible spatter

Note: Undoped CdS charge material used.
Molybdenum foil substrates, . 002" thick.

18

Electroformed metal mesh grids were tried, attaching them to the substrates in various ways. In a few cases just pressing the grids into the H-Film plastic with heat and pressure gave good results, but this method was difficult to control and for larger area cells there always seemed to be a portion of the grid that would peel back from the H-Film and thus would stick through the CdS layer during evaporation.

Some cells were fabricated with epoxy resin cement fastening the grids to the H-Film. While there was some small degree of success with this technique there were difficulties with the epoxy bleeding out from under the grids along the surface of the H-Film and causing difficulties with the adhesion of the CdS. A variation of this method used Pyre ML (liquid polyimide plastic) as the cement to hold down the grids to the H-Film substrate. Unfortunately, the Pyre ML appears to have poor adhesion to the grids after curing, though its adhesion to the H-Film is excellent.

Only 2 larger area backwall plastic substrate cells were successfully processed using the above techniques of cemented grids under the CdS layer. The results on these are summaried in Table IV.

TABLE IV
LARGE AREA BACKWALL CdS FILM CELLS ON PLASTIC SUBSTRATES

Cell No.	Active Area	OCV	SCC	Fill Factor	Efficiency
382	37. 8 cm^2	0. 43 V	13. 6 mA/cm^2	59%	3. 5%
384	33. 3	0. 36	12. 9	51	2. 4

Note: Nickel grids embedded or cemented to H-Film substrates. Silver print contact to barriers.

The embedded or cemented grids can probably be made to work and higher efficiency cells, possibly up to 4 to 6%, can probably be achieved. It has become evident, however, that a whole new technology must be acquired in order to do this, and that this will take more time than is presently available. Furthermore, this method of cell fabrication

19

is relatively expensive. More encouraging results are presently being obtained with the frontwall plastic substrate cell, and hence further work on the backwall substrate cell construction has been discontinued. It is planned to resume work on the backwall design at such time as the double layer CdS film is perfected and offers some hope of achieving higher efficiency cells without resorting to grids embedded in the substrate.

FRONTWALL PLASTIC SUBSTRATE CELL

a. Large Area Cells

Additional H-Film substrates with various evaporated gold coatings were received from the vendor, and the sheet resistance of these was about half what was received earlier and reported in the First Quarterly Report. However, these were set aside and not made into solar cells because much lower resistance substrates were prepared in our own laboratory.

A greatly improved conductive coating on the H-Film substrate was prepared by mixing a silver flake pigment in liquid Pyre ML varnish, spraying about a 5 micron thick layer onto H-Film with an artist's air brush, and curing in place. These coatings typically exhibit sheet resistances below 0.01 ohms per square, and are extremely adherent to the H-Film. The conductive coating is given a thin nickel plating prior to deposition of the CdS to ensure an ohmic contact.

These improved substrates made possible a standardization of a process for fabricating 3" x 3" frontwall cells. Improvements in the process were effected throughout the quarter. These improvements included improved homogeneity of the conductive coating by adequate milling of the silver-Pyre ML solution to break up agglomerates prior to spraying, elimination of dust attracted electrostatically to the H-Film, and generally improved processing techniques.

Twenty-two 3" x 3" cells were successfully fabricated through the process during the quarter and the results on these are listed in chronological order in Table V. The average cell efficiency was 3.0%, but the maximum was 4.4%, and as can be seen the last 5 cells are markedly better than those fabricated earlier. Particularly gratifying

20

TABLE V

LARGE AREA FRONTWALL CdS FILM CELLS ON PLASTIC SUBSTRATES

Cell No.	Area (cm^2)	OCV	SCC (mA/cm^2)	Fill (%)	Efficiency (%)
A412	44.5	0.48	12.3	41	2.5
A414	44.5	0.46	12.1	46	2.6
A417	38.6	0.46	11.3	57	2.9
A421	39.6	0.47	6.6	59	1.8
A422	33.4	0.48	12.3	61	3.6
A423	36.4	0.47	11.1	66	3.4
A424	37.9	0.46	8.3	62	2.3
A430	37.5	0.45	13.5	55	3.3
A431	41.2	0.41	7.1	58	1.7
A433	43.9	0.47	9.9	64	3.0
A434	42.5	0.47	14.0	62	4.1
A435	43.1	0.47	8.4	45	1.8
A439	41.5	0.46	9.6	66	2.9
A441	43.7	0.46	8.0	66	2.4
A445	39.9	0.48	9.5	64	2.9
A447	30.4	0.46	11.0	64	3.2
A464	38.4	0.47	10.8	65	3.3
A469	42.4	0.48	15.4	59	4.4
A471	46.0	0.46	15.6	50	3.4
A473	46.0	0.43	14.9	50	3.2
A476	45.7	0.47	16.8	54	4.3
A477	46.7	0.48	16.7	47	3.8
Avg.	41.1	0.46	11.6	57	3.0

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

is the short circuit current density of the last 5 cells which averaged 15. 9 mA/cm^2 and is nearly comparable with that of the frontwall metal substrate cell.

A fluctuation in the area of these cells arose from difficulties with pin holes and other flaws in some films. When these were detected visually they were blocked off from contact with the collector grid by the insertion of an insulating patch of plastic under the grid prior to lamination. Much of this type of difficulty has been traced to dust and grit particles that become embedded in the plastic films and cause flaws in the evaporated CdS layer.

Figure 4 shows the I-V characteristic curve of one of the better (4. 1% efficient) large area plastic substrate cells. It is evident that the output of this cell is not particularly limited by series or shunt resistance, but rather by the magnitude of the light generated current.

b.   Small Area Cells

A number of smaller area cells were constructed during the period using identical processing techniques. The only variations were that the films were completely unclamped during barrier formation (the smaller areas do not need to be clamped since they do not curl so severely), and minor variations in the conditions of barrier formation.

The results on these cells are summarized in Table VI. There was no correlation between the output of these cells and the conditions of the barrier formation process. Yet, these cells all gave higher short circuit current densities, lower open circuit voltages, and higher conversion efficiencies than the larger area cells listed in Table V. The average conversion efficiency of these smaller area cells was 4. 9% with a maximum of 5. 8%.

It appears that the improved output of the smaller area cells resulted from the fact that they were processed through barrier formation, heat treatment, and lamination, as small area cells rather than because they were tested as small area cells. Thus, when larger area cells processed through lamination were cut into smaller area cells and tested, their output was still comparable to the large area cells (on a

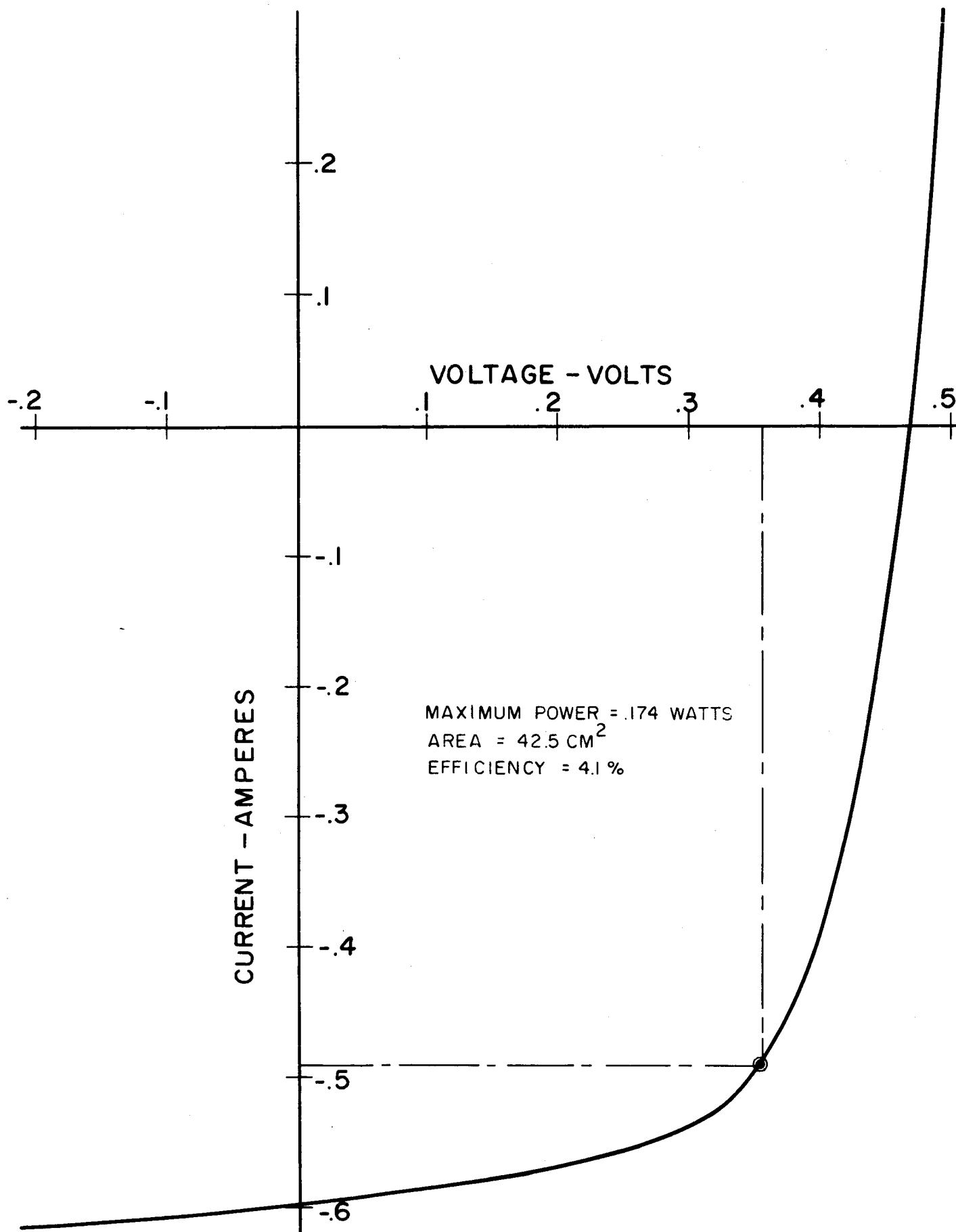CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

VOLTAGE – VOLTS

CURRENT – AMPERES

MAXIMUM POWER = .174 WATTS
AREA = 42.5 CM^2
EFFICIENCY = 4.1 %

FIG. 4. I-V CHARACTERISTIC OF LARGE AREA PLASTIC
SUBSTRATE CELL.

ERD 8017

TABLE VI

SMALL AREA FRONTWALL CdS FILM CELLS ON PLASTIC SUBSTRATES

Cell No.	Area (cm^2)	OCV (V)	SCC (mA/cm^2)	Fill (%)	Efficiency (%)
A426-1	2.7	0.42	15.8	57	3.8
A426-4	2.5	0.43	19.5	60	5.0
A426-5	2.9	0.43	20.6	45	4.0
A426-6	2.2	0.45	21.5	57	5.5
A426-7	2.5	0.45	19.5	57	5.0
A429-1	5.3	0.44	16.9	63	4.7
A429-5	6.8	0.41	17.2	53	3.8
A443-1	8.3	0.46	17.6	67	5.4
A443-2	7.4	0.47	19.8	62	5.8
A443-3	7.2	0.47	18.9	66	5.8
A443-4	4.8	0.45	19.2	53	4.6
Avg.	4.9	0.44	18.8	58	4.9

24

unit area basis) and not to the cells processed as small area cells.

Figure 5 shows the I-V characteristic curve of one of the 5. 5% efficient small area cells. It is evident that this is an appreciably poorer characteristic (i. e. , less rectangular) than that of the large area cell shown in Fig. 3. The difference clearly is that the higher efficiency smaller area cells produce more current per unit of cell area. It is not clear whether the larger area cells do not have as much short circuit current generated per unit area, or whether the currents are just not being collected. Further investigation is needed to understand this phe - nomenon.

FRONTWALL METAL SUBSTRATE CELL

a. Encapsulation Study

Frontwall metal substrate cells have depended on the plastic encapsulation to hold the electroformed metal mesh grid in pressure contact to the barrier. The standard encapsulant has been 2 mil thick clear "Mylar" plastic above and below the cell using 0. 5 mil thick "Capran" plastic as an adhesive. Fusing of the adhesive plastic is accomplished by heat (approximately 230°C) and pressure (approximately 100 psi) in a laminating die.

"Kapton" (polyimide) plastic film in 0. 5, 1. 0, and 2. 0 mil thicknesses has been employed in place of the "Mylar" to provide better resistance to ultraviolet and high energy particle radiation. The "Kapton" plastic provides a satisfactory encapsulation, though it is slightly more difficult to laminate than "Mylar". The main disadvantage is that it does not transmit the shorter wavelengths of light, and hence the initial output of a typical CdS frontwall cell is reduced about 20% because of this factor. It is presumed that the transmissive properties of the "Kapton" would not deteriorate noticeably in the space environment while those of "Mylar" and other clearer plastics would. Hence, after a period of time, on the order of 6 to 12 months in space, the "Kapton" encapsulated cells would retain their original output level while "Mylar" and other clear plastic encapsulated cells would degrade to levels below the "Kapton" cells.

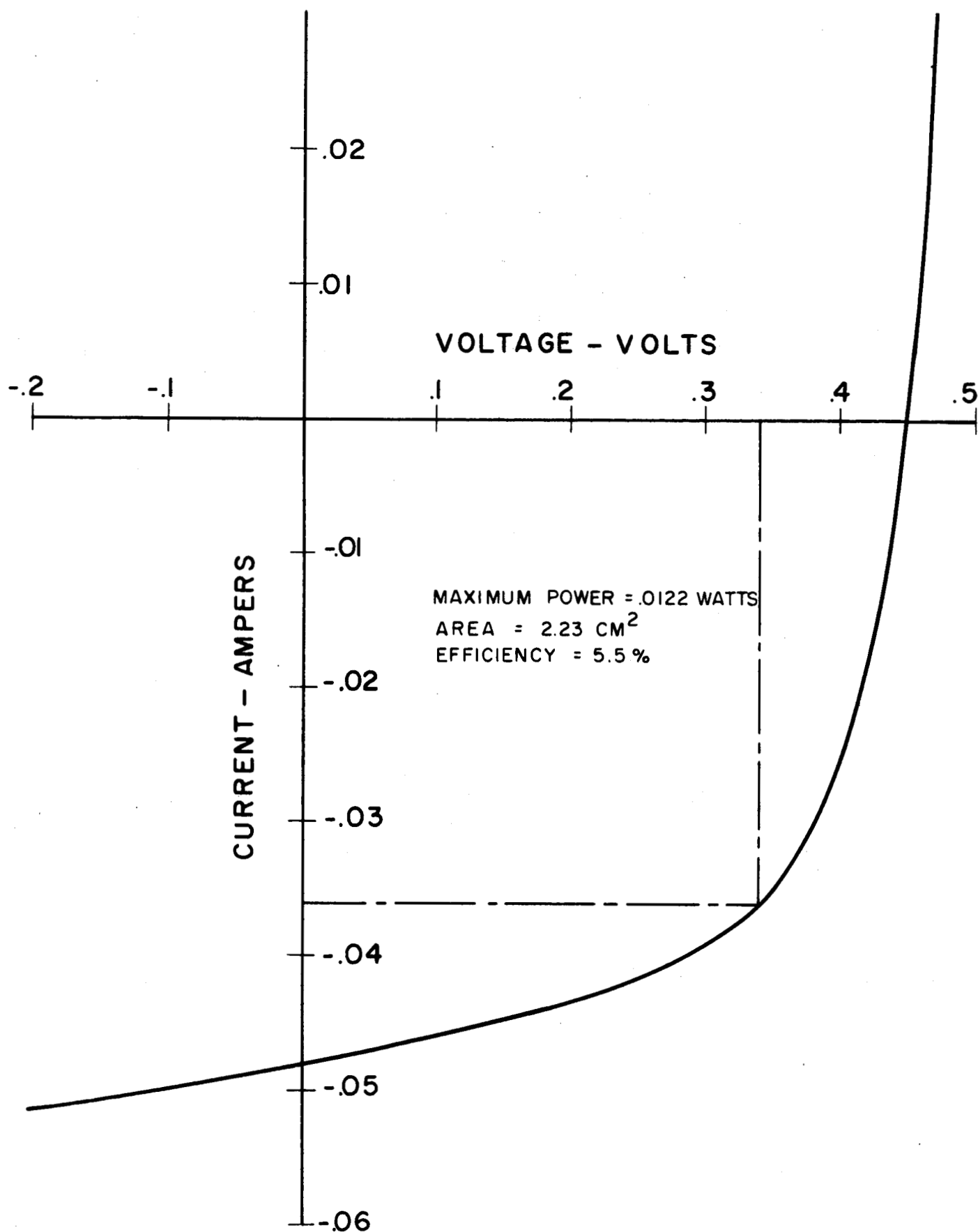CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

VOLTAGE – VOLTS

CURRENT – AMPERS

MAXIMUM POWER = .0122 WATTS
AREA = 2.23 CM^2
EFFICIENCY = 5.5 %

FIG. 5. I-V CHARACTERISTIC OF SMALL AREA PLASTIC
SUBSTRATE CELL.

ERD 8019

Neither the "Mylar" nor "Kapton" plastics are very imperme-
able to water vapor. Hence CdS cells encapsulated with these materials
do not withstand long periods of storage in moisture containing atmo-
spheres, or even short periods in extremely humid atmospheres. There
have been indications that the present design Clevite high efficiency CdS
film solar cells are more susceptible to moisture deterioration than
earlier design CdS solar cells with electroplated barriers.

A series of experiments were started to characterize the
properties of the present design CdS film solar cell with respect to
moisture damage. These experiments are intended to be preliminary to
a second series of experiments designed to improve the resistance of
the cells to moisture damage.

A glass enclosed chamber, maintained at 30°C, with air
at 80% relative humidity was chosen as a moderately severe environ-
ment for the purposes of this characterization.

A standard process 3" x 3" frontwall metal substrate CdS
film cell was chosen prior to lamination and cut into four pieces each
1 1/2" x 1 1/2". Two pieces were encapsulated in 14 mil "Mylar" one
in 2 mil "Mylar" and one in 10 mil "Kel-F". One of the 14 mil "Mylar"
encapsulated cells was placed in a desiccator at room temperature as a
control while the others were placed in the 80% humidity, 30°C, storage
chamber. All cells were tested after 1 week and after 2 weeks time.
The data are summarized in Table VII.

It is seen that the "Mylar" packaged cells exposed to the
severe humidity degraded to less than a tenth of their initial output
within a week, while the 10 mil "Kel-F" packaged cell degraded but at
a much slower rate. The desiccated cell on the other hand actually
improved its output slightly.

Efforts to revive the degraded cells were made by storing
them in vacuum at 100°C. After 1 month there has been no noticeable
increase in their efficiency. This is a distinct difference from observa-
tions on early design CdS single crystal solar cells which could be com-
pletely recovered from moisture degradation by vacuum or desiccated
atmosphere storage.

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

TABLE VII

MOISTURE DEGRADATION TEST OF VARIOUS ENCAPSULANTS

Cell No.	B 366A I	B 366A II	B 366A III	B 366A IV
Encapsulation	14 mil Mylar	14 mil Mylar	2 mil Mylar	10 mil Kel-F
Storage	Desiccator 25°C	80% R. H. 30°C	80% R. H. 30°C	80% R. H. 30°C
Initial Efficiency	5. 8%	5. 5%	5. 5%	6. 2%
Efficiency after 7 days	5. 8%	< 0. 5%	< 0. 5%	5. 3%
Efficiency after 14 days	6. 2%	< 0. 5%	< 0. 5%	4. 8%

28

b. Stability on Temperature Cycling

Some of the special construction cells that were described in the First Quarterly Report on this contract were delivered to the Energy Conversion Laboratory of the Lewis Research Center, NASA, where they were tested on their vacuum thermal cycling test. This test is designed to simulate on an accelerated basis the variation in temperature expected to be experienced by a thin film solar cell array in earth orbit.

Four of the frontwall metal substrate cells with conductive epoxy cemented grids (two with gold grids and two with copper grids) were placed on test. All of these cells degraded rapidly to about 25% of their initial output in the first 100 temperature cycles, then levelled off and showed no further degradation as of 1500 cycles at the time of this writing. There is no indication of any short circuiting of these cells occurring, such as has been experienced on some frontwall cells where the grids have been held in pressure contact to the barrier by the plastic encapsulation.

The steady degradation of these cells on vacuum thermal cycling is a new experience. It appears to be similar to what occurs when cells are exposed to moisture, or what might be expected if cell barriers were exposed to traces of tri-valent cation impurities. The conductive epoxy cement used to attach the grids to the barriers of these cells was a standard commercial product. There was no attempt made to remove any possible absorbed moisture or air, and epoxies generally seen to absorb substantial amounts of air and moisture. Also, these filled epoxies are not generally considered to be of extremely high purity. Thus, there is a real probability that some deleterious ingredient or contaminant in the cement was responsible for the degradation of the cells. Additional work is planned with conductive cementing of grids in an attempt to determine and eliminate the factor causing cell degradation.

In addition, two plastic substrate cells were placed on vacuum thermal cycling test. Cell No. 368H was an H-Film ("Kapton") substrate

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

cell fabricated as a frontwall-backwall combination cell, and cell No. 374H was a frontwall plastic substrate cell using an evaporated gold coating on the plastic. Both of these cells have withstood 1500 temperature cycles as of this writing, with no indications of any short circuits developing. The output of the frontwall-backwall cell has dropped to about 90% of its output at the beginning of temperature cycling, while the frontwall cell is well above 90% of its initial output.

c. Grid Design

Electroformed gold mesh grids are being used to collect the current from the barrier layer of the frontwall thin film solar cell. These grids are very expensive and very delicate to handle in production. There have been indications also that the grids may be limiting the output of the very high efficiency cells.

Earlier in-house work established that electroformed copper grids give equivalent cell efficiencies. The copper grids are somewhat less expensive, and they are easier to handle than the gold grids. Substitution of copper for gold on the "standard" cell construction has been held up however, pending further information on the longer term stability of cells with copper grids.

The grids used are 60 line per inch grids with a square mesh pattern giving approximately 85% open area. The grids are about 0.5 mils in thickness and both copper and gold grids appear to have about the same value of sheet resistance which is 0.03 ohms per square. At present the standard 5% 50 cm^2 area frontwall metal substrate cells have a total equivalent series resistance in the range of 0.06 to 0.10 ohms. The resistance of a 3" x 3" grid as seen by the cell should be about half of its sheet resistance, or in this case about 0.015 ohms.

In 140 mW/cm^2 sunlight, a 3" x 3" cell of 5% conversion efficiency should have a current output of about 1 ampere at maximum power transfer. This represents a power loss of 15 milliwatts in an 0.015 ohm resistive grid or a reasonably negligible proportion (4%) of the total 350 mW power output. Even the loss in a 7% 3" x 3" cell is not too severe (about 6% of the total power output) as long as the grid resistance

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

remains at 0. 015 ohms. If however, the grid resistance were to increase
to 2 or 3 times its present value, the power loss in the grid would no
longer be negligible, but could drop the output of an otherwise 7% cell
to well below 6% at the output terminals. Therefore the grids actually
received are being carefully checked to ensure that they remain low in
resistance.

Some work has been started to develop a new grid design
that will combine as much as possible a maximum of electrical conductivity
with a minimum loss of light transmission and at the same time will be
economical and easy to handle. A grid with more "wires" running in one
direction than in the other should be more advantageous than the present
square mesh pattern. The design of such a pattern grid is being worked
out at present based upon earlier preliminary work. Some difficulties
are being encountered in laminating revised design grids due to such
factors as gas entrapment, grid wire breakage, and intimacy of contact
of the grid to the barrier surface.

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION

REFERENCES

1. R. W. Aldrich and D. A. Cusano "Research on Thin Film Poly-crystalline Solar Cells, " AFAPL Technical Report 65-8 (February, 1965).

2. F. A. Shirland, G. A. Wolff and J. D. Nixon "Research on Solar-Electrical Energy Conversion, " ASD Technical Documentary Report 62-69, Vol. I, (January, 1962).

3. R. R. Chamberlin and J. S. Skarman "Feasibility Investigation of Chemically Sprayed Thin Film Photovoltaic Converters, " ASD Technical Documentary Report 63-223, Part II, (October, 1963).

CLEVITE CORPORATION   ELECTRONIC RESEARCH DIVISION